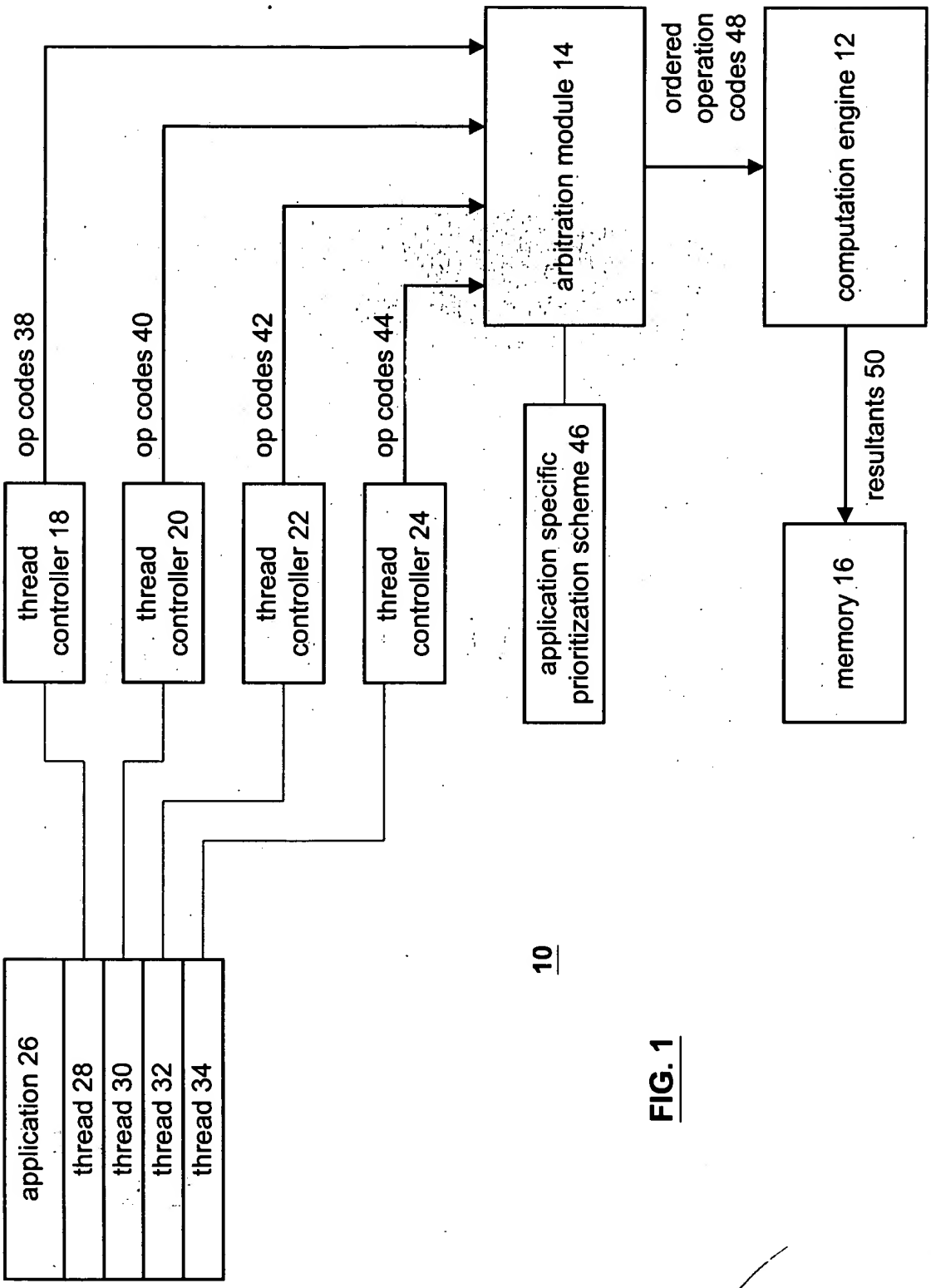


FIG. 1

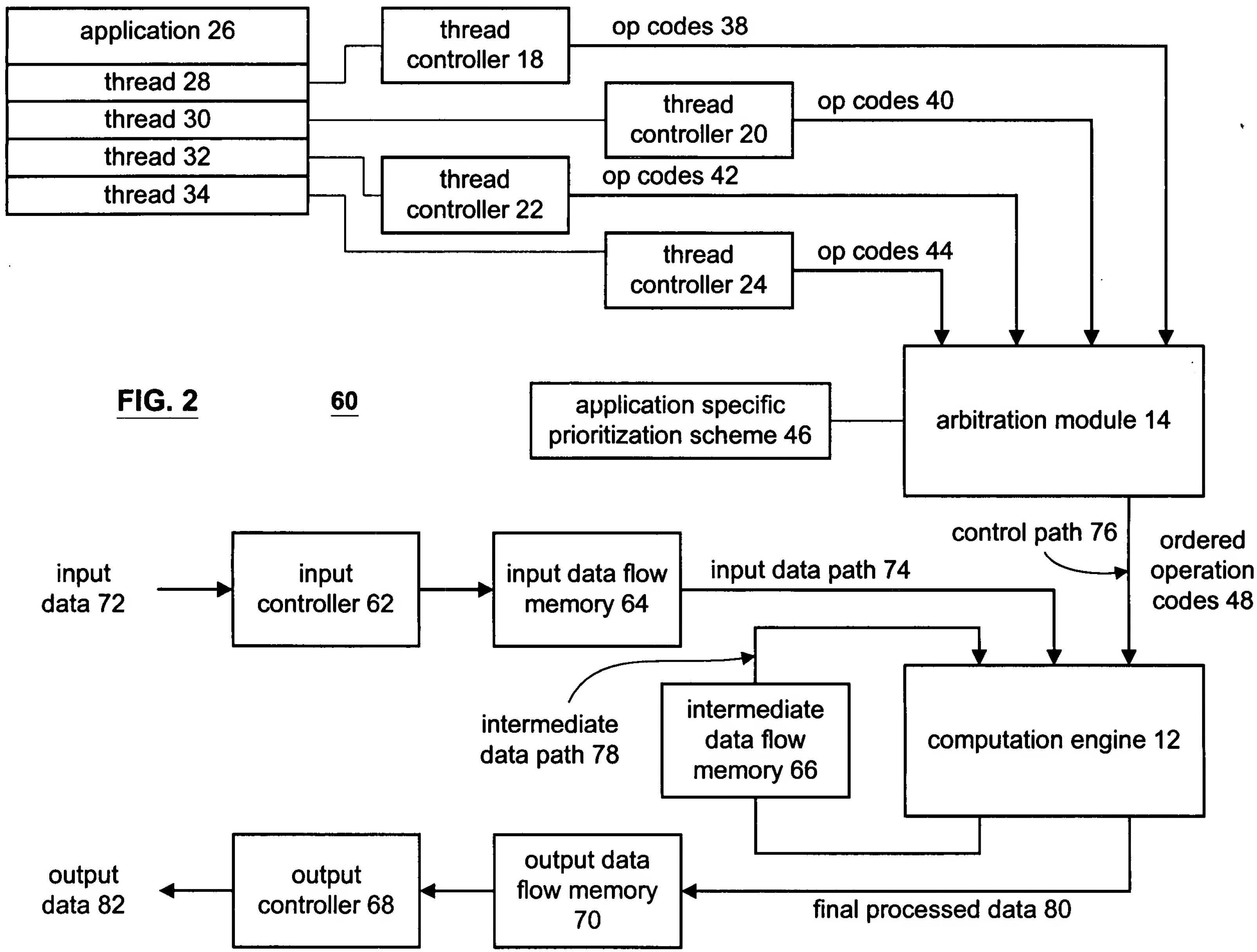

application 26
thread 28
thread 30
thread 32
thread 34
thread controller 18
thread controller 20
thread controller 22
thread controller 24
op codes 38
op codes 40
op codes 42
op codes 44
60
application specific prioritization scheme 46
arbitration module 14
control path 76
ordered operation codes 48
input data 72
input controller 62
input data flow memory 64
input data path 74
intermediate data path 78
intermediate data flow memory 66
computation engine 12
output data 82
output controller 68
output data flow memory 70
final processed data 80

FIG. 2

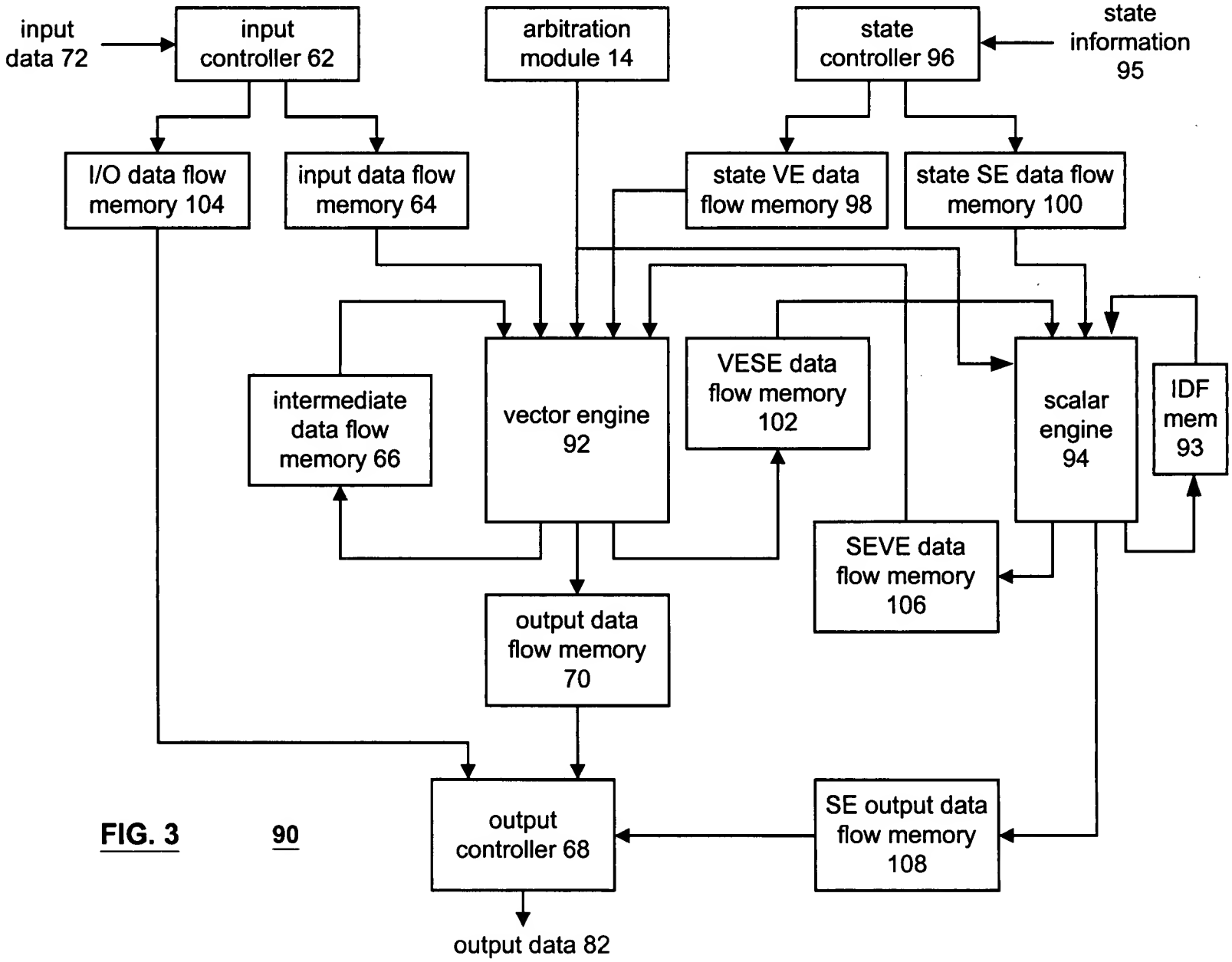


FIG. 3 90

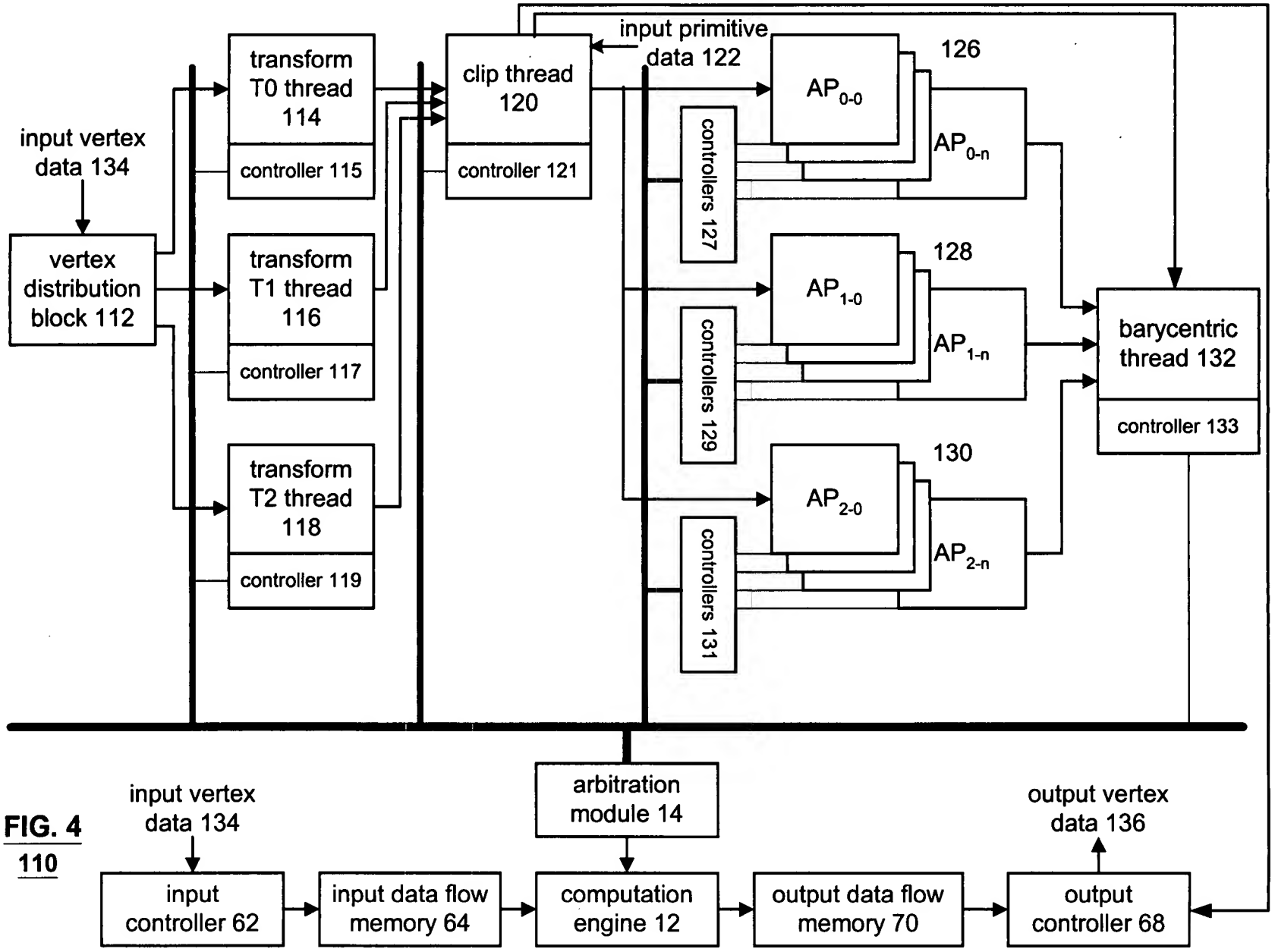

input vertex data 134
vertex distribution block 112
transform T0 thread 114
controller 115
transform T1 thread 116
controller 117
transform T2 thread 118
controller 119
clip thread 120
controller 121
input primitive data 122
controllers 127
controllers 129
controllers 131
AP0-0
AP0-n
AP1-0
AP1-n
AP2-0
AP2-n
126
128
130
barycentric thread 132
controller 133
arbitration module 14
input vertex data 134
input controller 62
input data flow memory 64
computation engine 12
output data flow memory 70
output controller 68
output vertex data 136
110

FIG. 4

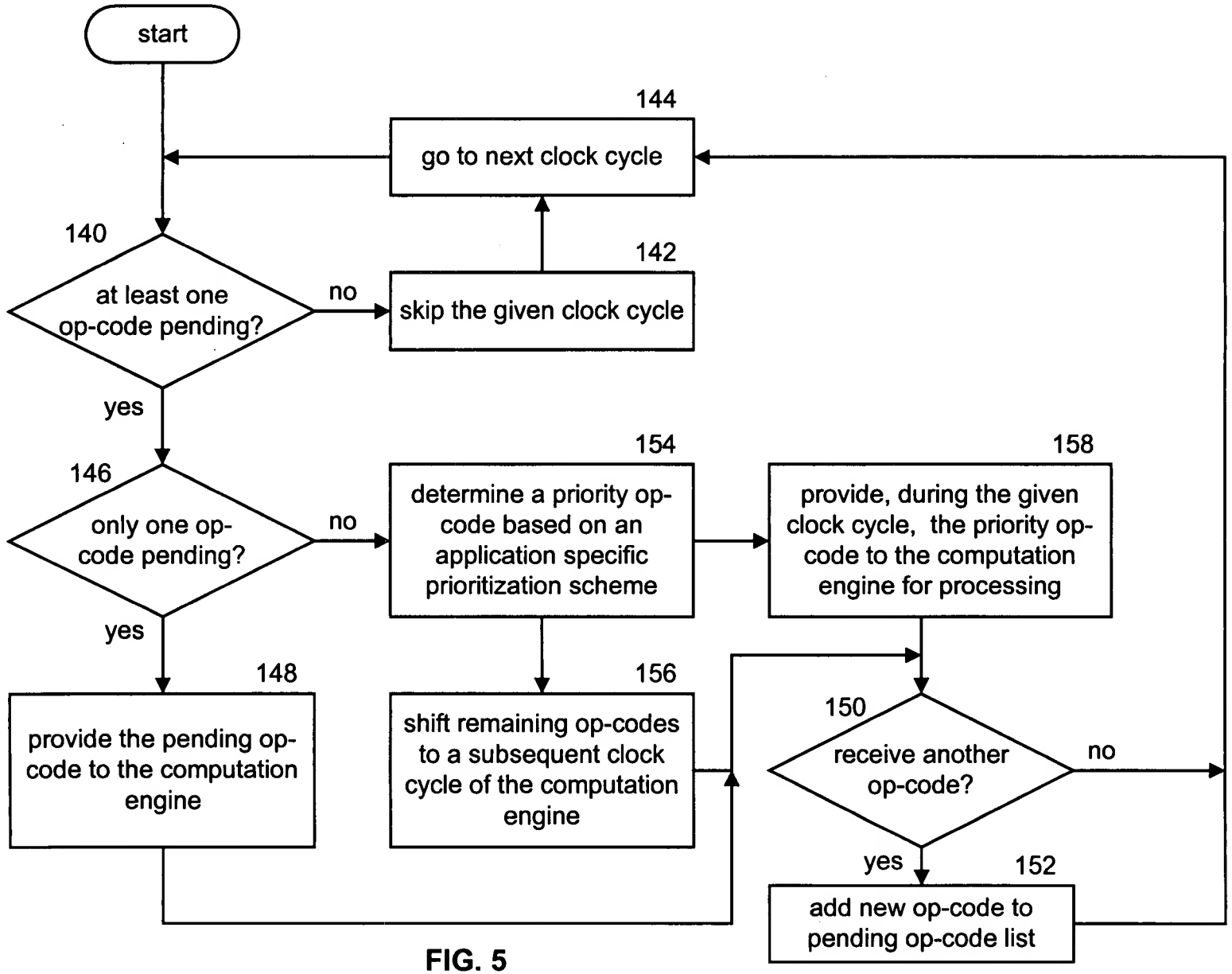


FIG. 5

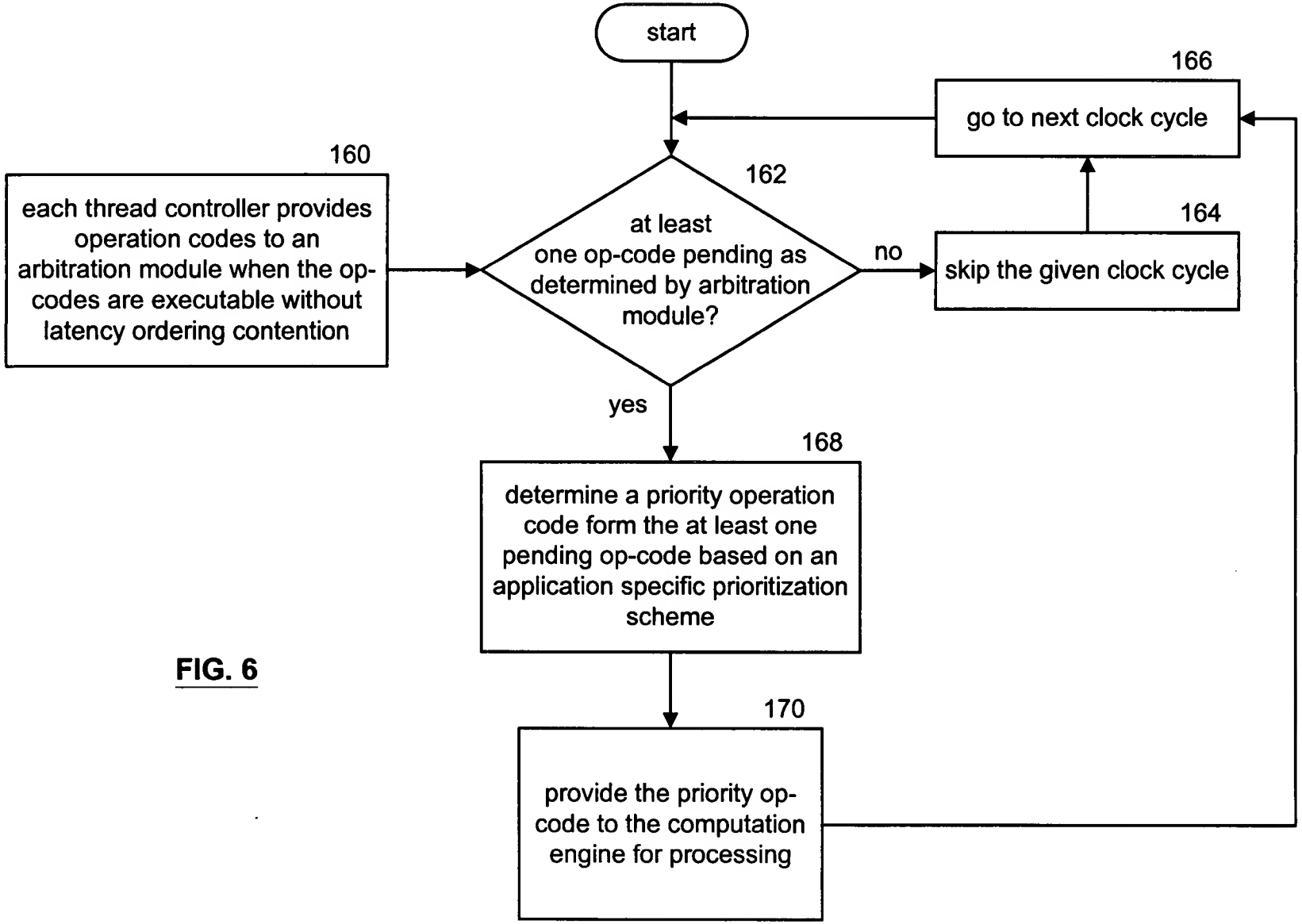


FIG. 6

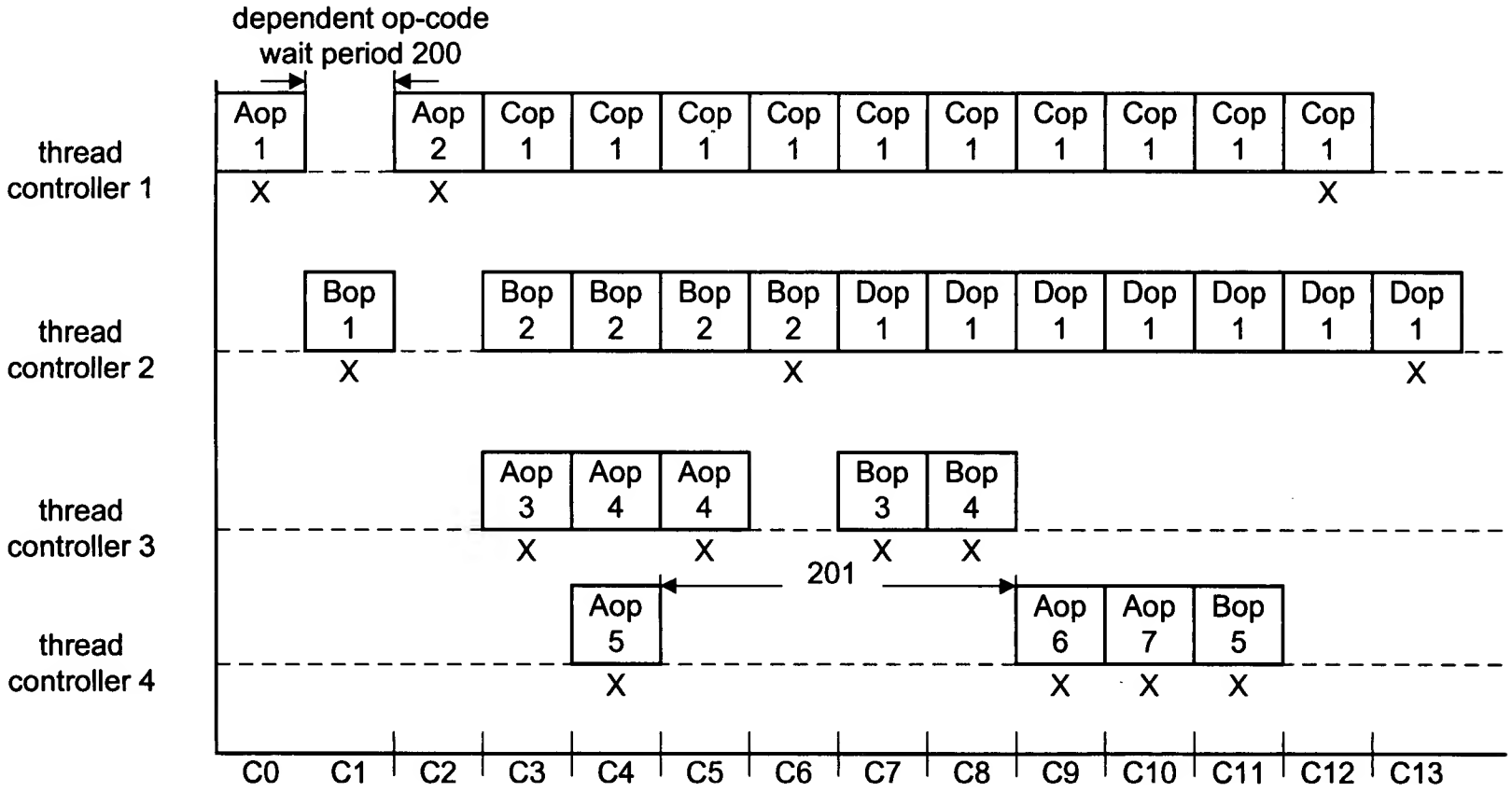


FIG. 7

prioritization scheme
thread 4
thread 3
thread 2; thread 1

X indicates selected by arbitration module based on priority scheme

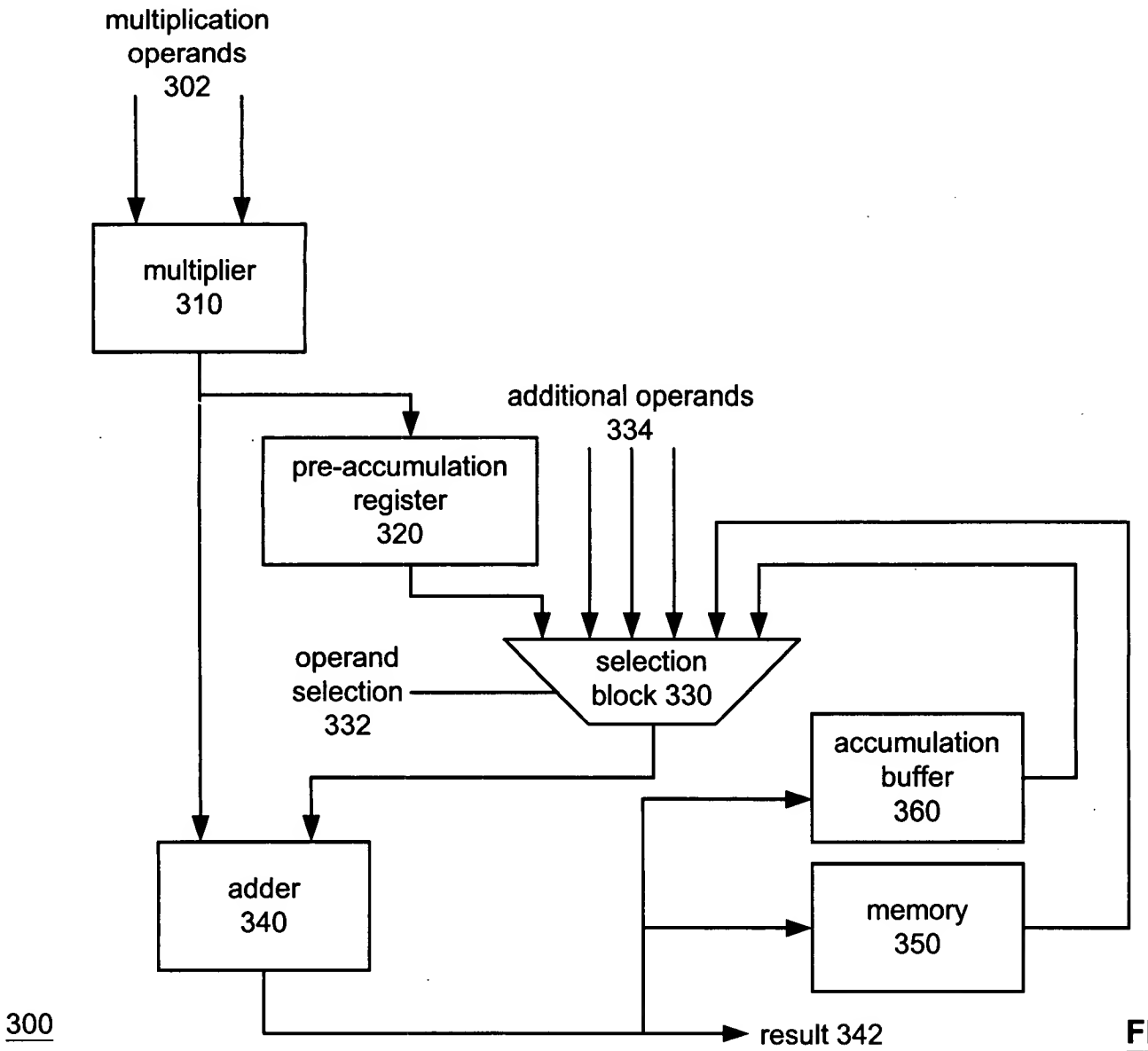


FIG. 8

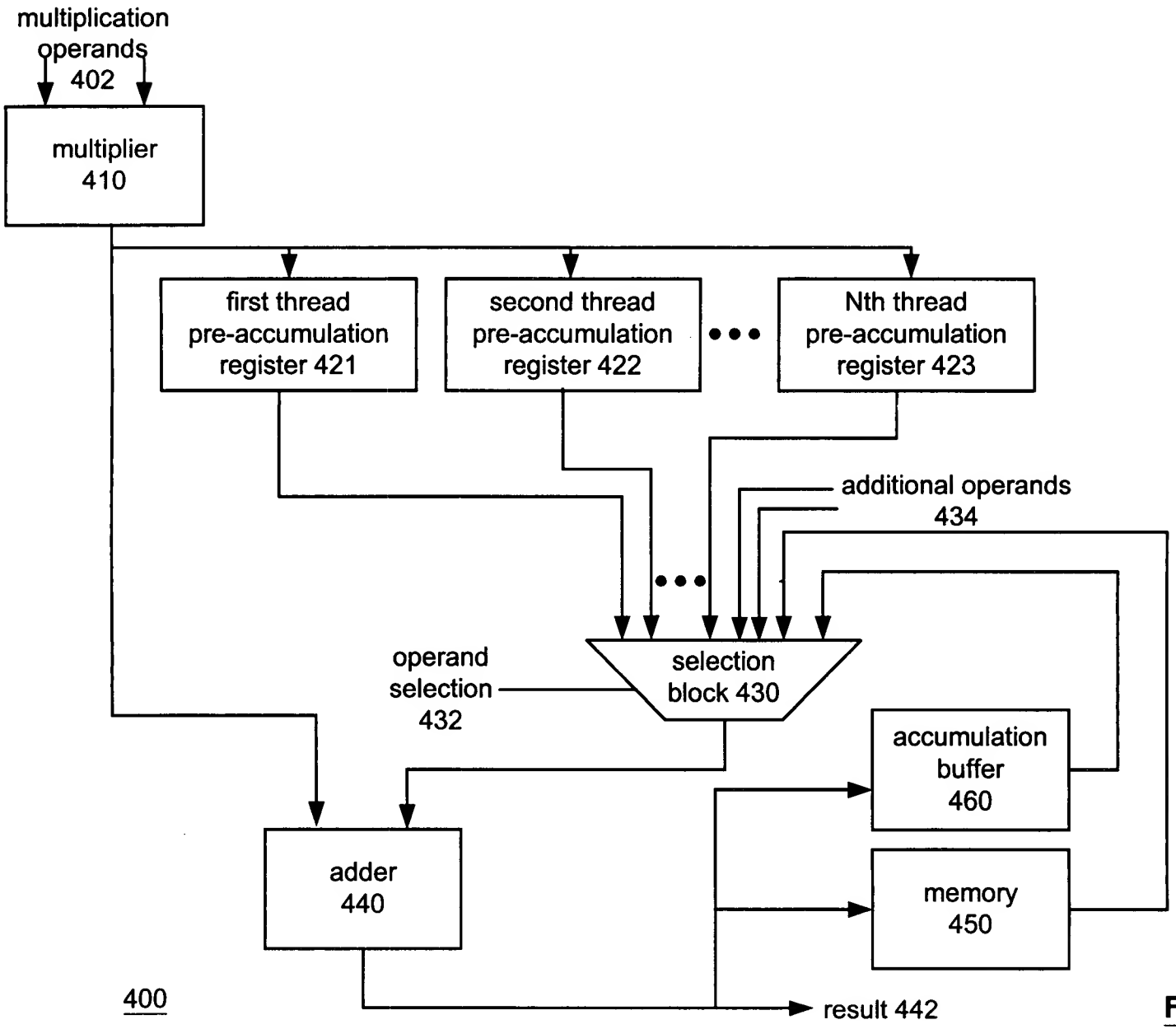

multiplication operands 402
multiplier 410
first thread pre-accumulation register 421
second thread pre-accumulation register 422
Nth thread pre-accumulation register 423
additional operands 434
operand selection 432
selection block 430
accumulation buffer 460
adder 440
memory 450
result 442
400

FIG. 9

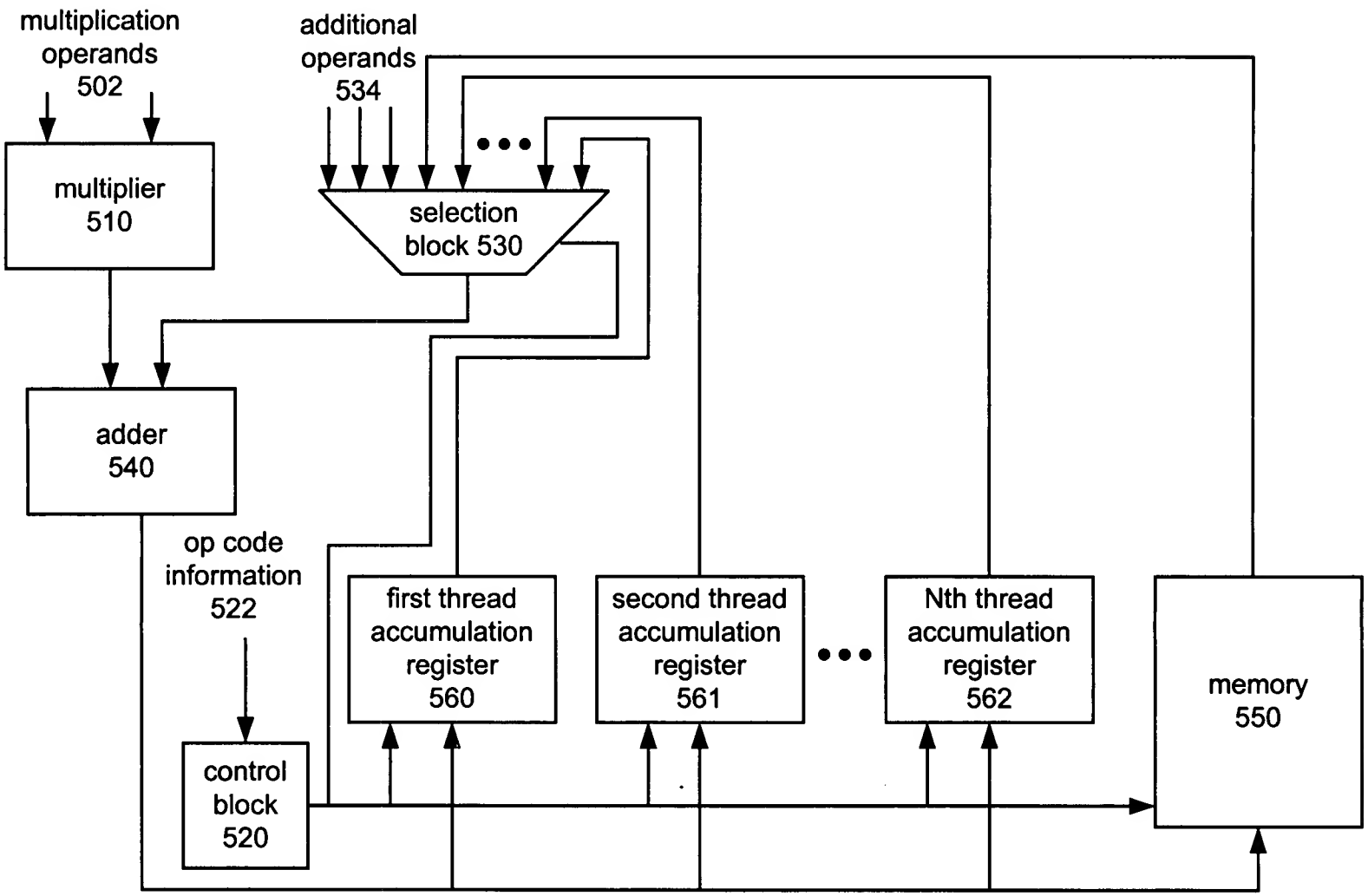


FIG. 10

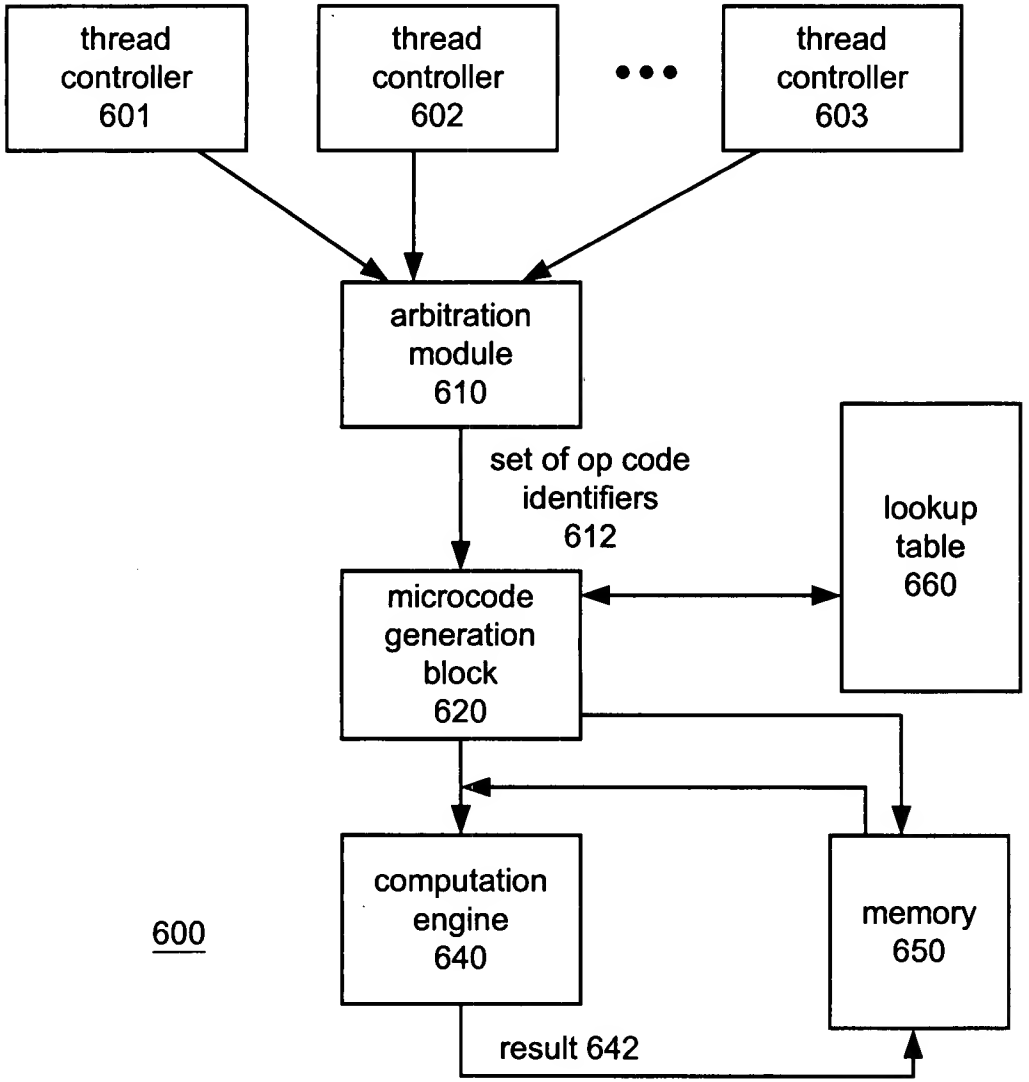


FIG. 11

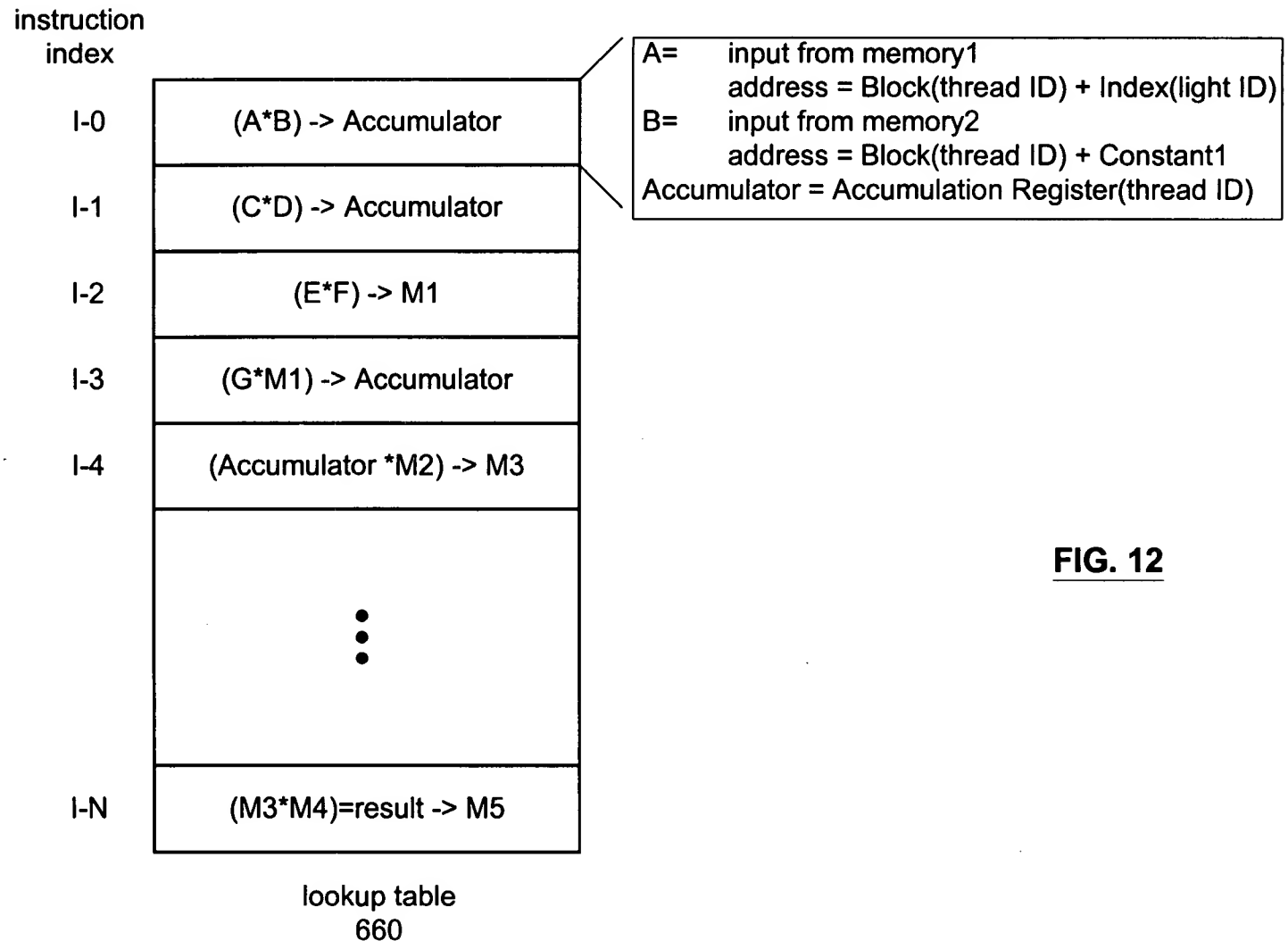
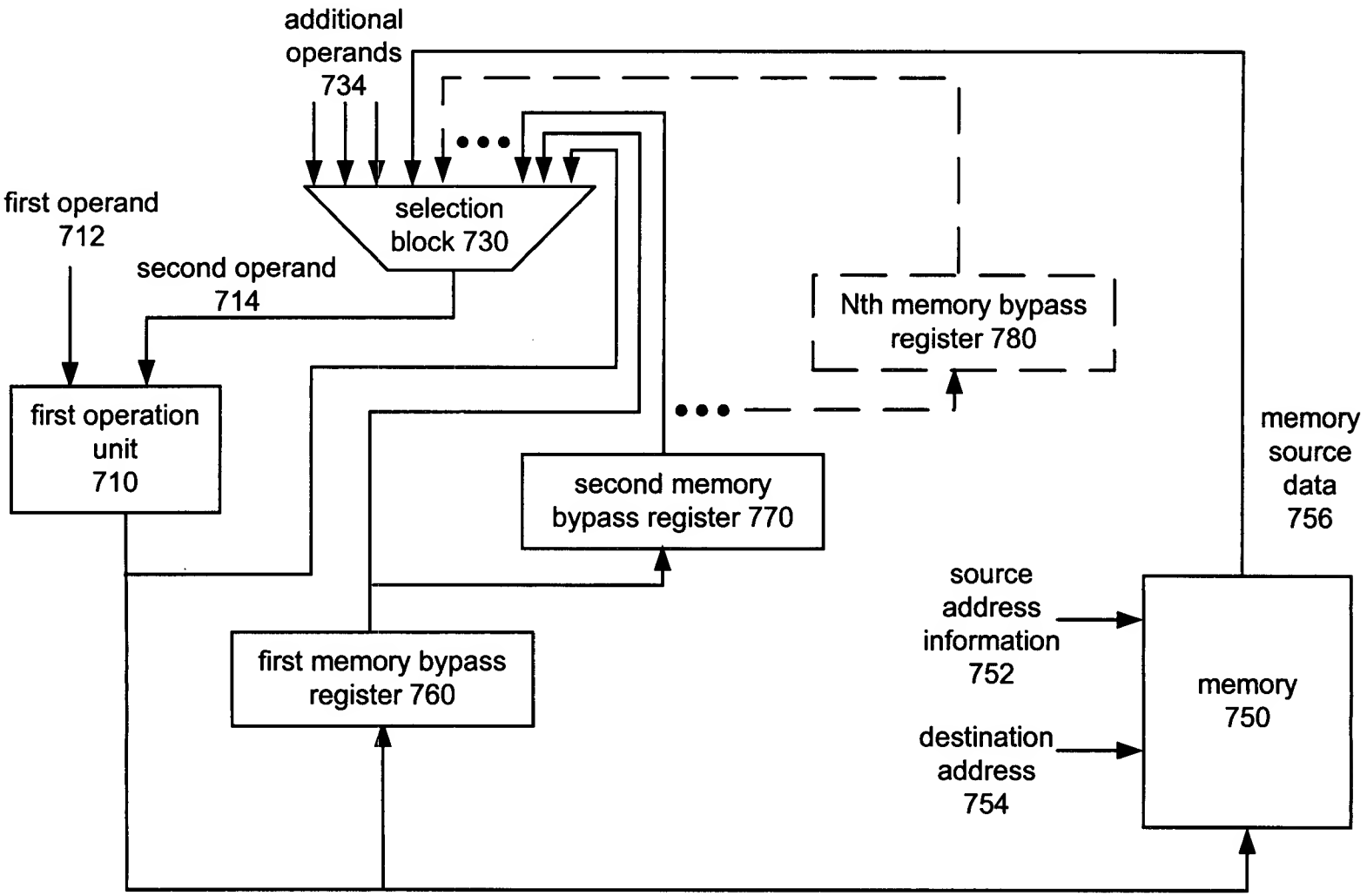


FIG. 12



700

FIG. 13

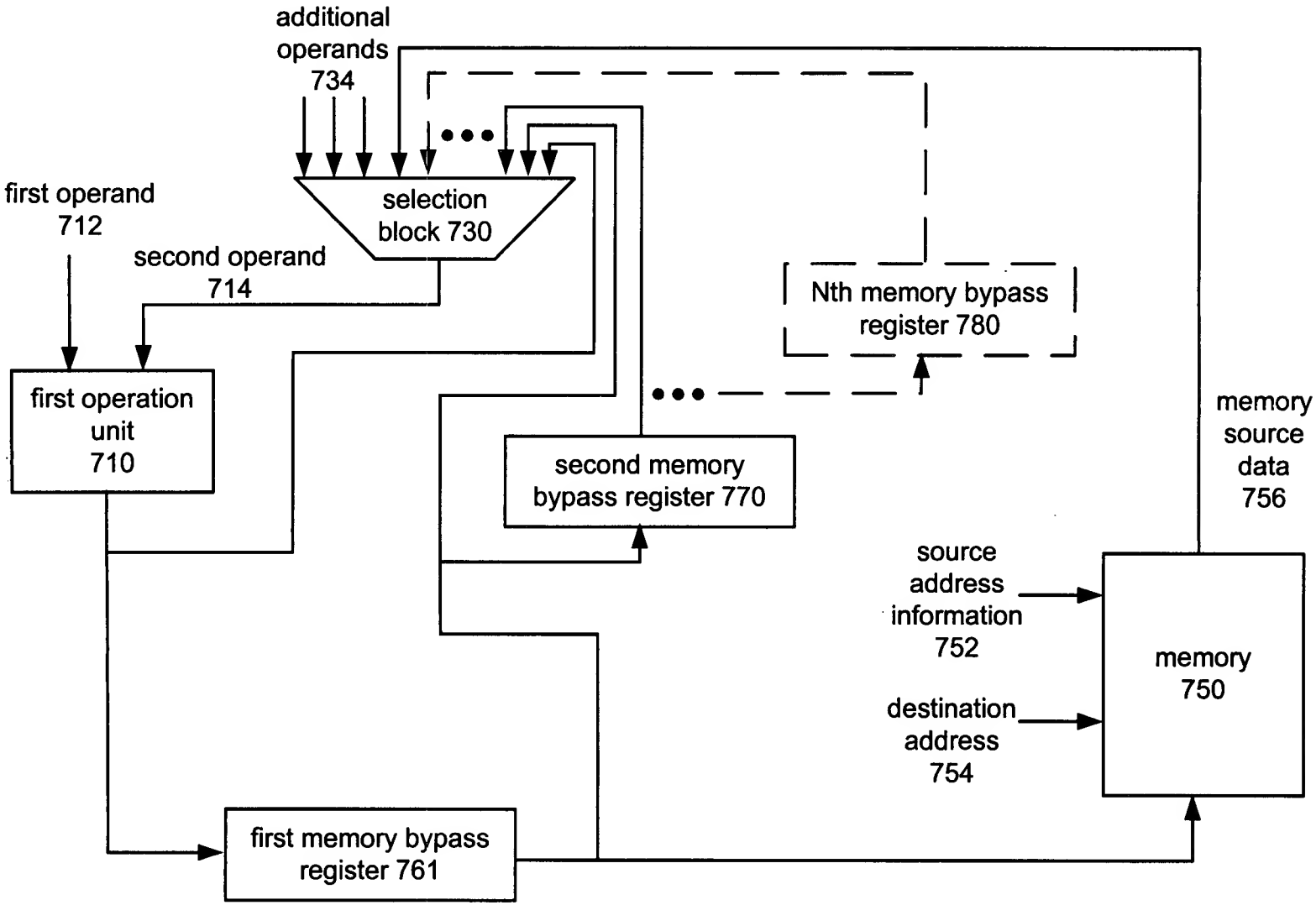
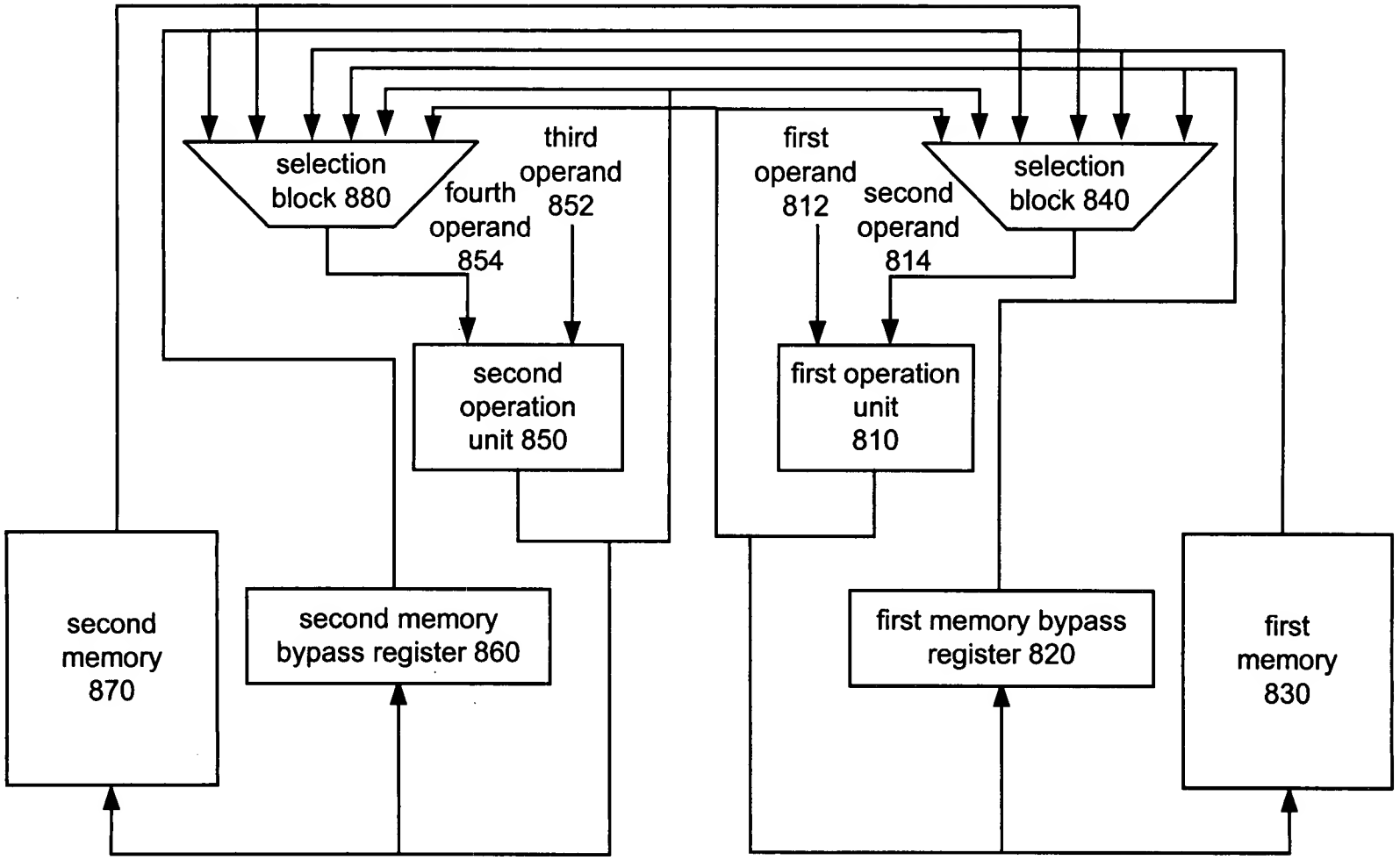

additional operands 734
first operand 712
second operand 714
selection block 730
Nth memory bypass register 780
first operation unit 710
second memory bypass register 770
memory source data 756
source address information 752
destination address 754
memory 750
first memory bypass register 761
701

FIG. 14


selection block 880
third operand 852
fourth operand 854
first operand 812
second operand 814
selection block 840
second operation unit 850
first operation unit 810
second memory 870
second memory bypass register 860
first memory bypass register 820
first memory 830

800

FIG. 15